Claims

1. (Previously presented) A method comprising:

retrieving state configuration information from a state server of a hardware/software co-simulation, the hardware/software co-simulation comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;

a first kernel managing access to the memory store; and

a second kernel comprising a co-simulation manager and a memory manager; and

providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.

2. (Original) The method of claim 1 wherein the state server defines an address space or a virtual address space in the hardware/software co-simulation.

3. (Canceled)

4. (Original) The method of claim 1 further comprising:

registering the client with a co-simulation interface; and

associating the client with at least one state server in the hardware/software co-simulation.

5. (Original) The method of claim 4 wherein registering the client comprises assigning the client a client identifier.

6. (Original) The method of claim 4 wherein associating the client with at least one state server comprises providing the client with a list of available state servers and one or more address spaces associated with each of the available state server.

7. (Original) The method of claim 6 wherein said client is to retain an identifier for at least one address space from the list.

8. (Original) The method of claim 6 wherein said client is to return a selection from the list and wherein associating the client with at least one state server further comprises providing the client an identifier for at least one address space from the list based on the selection.

9. (Canceled)

10. (Original) The method of claim 1 further comprising:

requesting the state configuration information, said state configuration information to define at least one memory location comprising the server state.

11. (Original) The method of claim 10 wherein requesting the state configuration information comprises:

receiving a client identifier for the client at a co-simulation interface;

receiving an identifier for an address space at the co-simulation interface, said server state being within the address space; and

issuing a request from the co-simulation interface, said request including the client identifier and the identifier for the address space.

12. (Original) The method of claim 11 wherein the request is to be serviced by the state server, said state sever to access a symbol table indicated by the identifier for the address space and to provide the state configuration information based on the symbol table.

13. (Previously presented) The method of claim 11 where a path of the request comprises an interprocess connection and a debugger.

14. (Original) The method of claim 1 wherein providing the client access comprises:

performing a memory operation on at least one memory location based on the state configuration information.

15. (Original) The method of claim 14 wherein performing the memory operation comprises at least one of:

reading the server state;

modifying the server state;

receiving the server state at a predetermined future time; and

receiving notification upon a predetermined action on the server state.

16. (Original) The method of claim 14 wherein performing the memory operation comprises:

generating a request for the memory operation, said request including a memory allocation from the state configuration information;

accessing a memory map; and

issuing the memory operation to a unified memory for the hardware/software co-simulation based on the memory allocation and the memory map.

17. (Original) The method of claim 16 further comprising:

receiving data in response to the memory operation; and

interpreting the data based on a symbol type defined by the state configuration information.

18. (Original) The method of claim 1 further comprising:

receiving stimulus based on the server state; and

applying the stimulus to the hardware/software co-simulation.

19. (Original) The method of claim 18 wherein the stimulus comprises data to be injected into the hardware/software co-simulation in response to a predetermined condition associated with the server state.

20. (Previously presented) A method comprising:

accessing a software state from a hardware simulation process in a hardware/software co-simulation, the hardware/software co-simulation comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;

a first kernel managing access to the memory store; and

a second kernel comprising a co-simulation manager and a memory manager; and

providing access to the software state to a client of the hardware/software co-simulation.

21. (Previously presented) A machine readable storage medium having stored thereon machine executable instructions, execution of said machine executable instructions to implement a method comprising:

retrieving state configuration information from a state server of a hardware/software co-simulator, the hardware/software co-simulator comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;

a first kernel managing access to the memory store; and

a second kernel comprising a co-simulation manager and a memory manager; and

providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.

22. (Previously presented) A machine readable storage medium having stored thereon machine executable instructions, execution of said machine executable instructions to implement a method comprising:

accessing a software state from a hardware simulation process in a hardware/software co-simulation, the hardware/software co-simulation comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;

a first kernel managing access to the memory store; and

a second kernel comprising a co-simulation manager and a memory manager; and

providing access to the software state to a client of the hardware/software co-simulation.

23. (Previously presented) An apparatus comprising:

a hardware/software co-simulator to retrieve state configuration information from a state server, the hardware/software co-simulator comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;

a first kernel managing access to the memory store; and

a second kernel comprising a co-simulation manager and a memory manager; and

a unified memory store, said hardware/software co-simulator to provide a client access to a server state of the state server within the unified memory store based on the state configuration information.

24. (Canceled)

25. (Canceled)

26. (Original) The method of claim 1, wherein the memory mapping comprises a plurality of memory addresses corresponding to the server state.

27. (Original) The method of claim 26, wherein providing comprises:

accessing a plurality of memory locations based on the plurality of memory addresses corresponding to the server state;

assembling a plurality of data bits occupying the plurality of memory locations; and

interpreting the assembly of the plurality of data bits based at least in part upon the symbol type.

28. (Original) The method of claim 1, wherein the state server comprises at least one component that contains and allows for exporting of the state configuration information to the client.

29. (Original) The method of claim 1, wherein the state server comprises a hardware process.

30. (Original) The method of claim 1, wherein the state server comprises a software process.

31. (Original) The method of claim 16, wherein the memory map maps at least one address corresponding to the simulation of the at least one memory device.

32. (Original) The method of claim 16, wherein the memory map represents a plurality of address spaces.

33. (Original) The method of claim 1, wherein the memory interface model represents input and output behavior of the at least one memory device.

34. (Original) The method of claim 1, wherein the simulation of the microprocessor comprises simulation at least in part by a first instruction set simulator.

35. (Original) The method of claim 34, wherein the first bus interface model represents input and output behavior of the simulation of the microprocessor.

36. (Original) The method of claim 34, wherein the co-simulation manager monitors transactions between the first instruction set simulator and the first bus interface model.

37. (Original) The method of claim 1, wherein the first kernel and second kernel are the same kernel.

38. (Original) The method of claim 34, wherein the hardware/software co-simulation further comprises a simulation of a digital signal processor, the digital signal processor having a corresponding address space and a corresponding symbol table.

39. (Original) The method of claim 38, wherein the simulation of the digital signal processor comprises simulation at least in part by a second instruction set simulator and a second bus interface model.

40. (Original) The method of claim 34, wherein the hardware/software co-simulation further comprises a simulation of a generic co-simulation client, the generic co-simulation client having a corresponding address space and a corresponding symbol table.

41. (Original) The method of claim 40, wherein the generic co-simulation client is simulated by a second instruction set simulator and a second bus interface model.

42. (Original) The method of claim 1, wherein the memory manager manages access to the memory store by the second kernel.